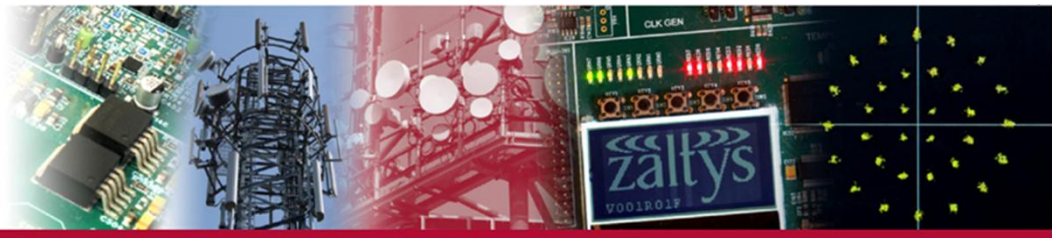

High Data Rate Demodulator Core

HDRM-D
HDRM-D2

Introduction

The Zaltys High Data Rate Demodulator (HDRM-D) and the Zaltys Enhanced High Data Rate Demodulator (HDRM-D2) IP cores efficiently realize the digital baseband section of a high performance modem receive path, including quasi-zero IF to baseband conversion, sample decimation, symbol timing recovery, and carrier recovery.

The Zaltys High Data Rate Demodulator (HDRM-D) IP core can demodulate BPSK, QPSK, offset-QPSK (OQPSK), 8PSK and 16QAM modulation schemes, all to a high performance level and at high symbol rates. The demodulator is highly flexible, supporting continuously variable software-selectable symbol rates of between 4.9kbaud and 40Mbaud, when operating with a fixed 100MHz system/ADC clock rate.

The Zaltys Enhanced High Data Rate Demodulator (HDRM-D2) IP core can additionally demodulate 8QAM (3 shapes), 32/64QAM &16/32APSK, and contains an adaptive equaliser to reduce linear channel distortion such as multipath. It also offers the option of increased datapath resolution to help cope with elevated levels of adjacent carrier interference.

Applications

The HDRM-D and HDRM-D2 cores are ideally suited to point-to-point wireless applications such as satellite communications and microwave line-of-sight backhaul links (e.g. for cellular, broadband or WiMAX). They also have applications in wired and optical links.

Features

- Versatile digital demodulation engine supporting BPSK, QPSK, offset-QPSK (OQPSK), 8PSK, 8QAM* (three variants), 16QAM, 32/64QAM* & 16/32APSK*
- Close to theoretical performance
- Option to increase datapath resolution to help cope with elevated levels of adjacent carrier interference*
- N-stage symbol rate blind adaptive equaliser option reduces linear channel distortions such as multipath*
- Supports continuously variable symbol rates
- Internal filter decimates up to a factor of 4096
- Supports typical rates of 4.9kbaud to 40Mbaud with 100MHz clock (range scales linearly with clock)
- Four matched filter configurations with alphas of 20%, 25%, 35% & 40% (others available on request)
- Fast acquisition algorithm
  - Combined coarse/fine frequency scan
  - High probability of first pass acquisition
- Highly configurable and versatile - fully programmable via simple microprocessor interface (SMPI)
- Fully programmable dynamic operation
  - Independent acquisition & track parameters
  - Configurable timing & carrier lock characteristics
- 10 to 14-bit I & Q datapath/ADC interface resolution*
- Constellation output interface suitable for connecting to soft-decision forward error correction (FEC)
- AGC control interface to analogue front-end
- Status interface reports real-time demodulation state
- Comes with software driver in C
- Extensive support for software monitoring
- Suitable for FPGA or ASIC implementation
- Synchronous design with single clock
- Hardware evaluation board (available extra)

**HDRM-D2 core only*

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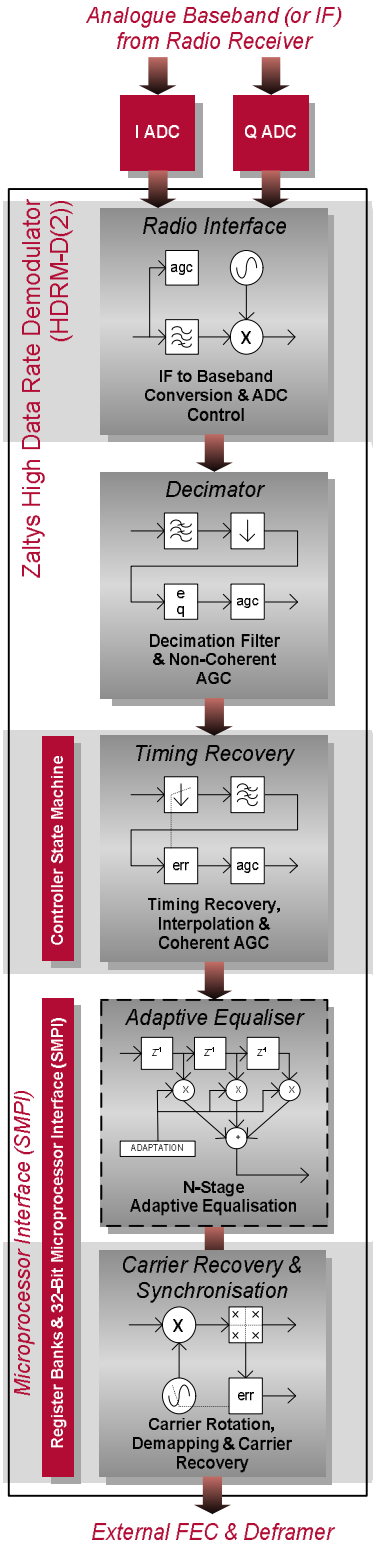
High Data Rate Demodulator Core



Technical Overview

In order to deliver performance close to the theoretical limits, the design utilizes multiple gain control stages within the data path to maximize dynamic range. Up to four sets of matched root-raised cosine filter coefficients can be incorporated into a given implementation, allowing four excess bandwidth values for the input signal to be selected in software. All aspects of the timing and carrier recovery are fully programmable, including loop filter coefficients and lock detector thresholds. In addition, monitoring registers provide a high degree of software visibility for parameters such as frequency offsets, lock levels and SNR estimation. The primary demodulator output is a sequence of symbols, nominally positioned at the specified constellation points. This allows a soft-decision forward-error-correction function to be easily used with this demodulator. Additional outputs include an I & Q monitor feature, which can be used to either view the constellation (via an external DAC), or alternatively, to carry hard-sliced data.

The demodulator datapath consists of five distinct sections. These correspond to the Radio Interface, Decimator, Timing Recovery, Adaptive Equaliser* and Carrier Recovery functions. The overall operation of the system is automatically managed by an integrated Finite State Machine controller. Communications with the core is handled by a 32-bit Simple Microprocessor Interface (SMPI).

The **Radio Interface (RIF)** block converts from quasi-zero IF to baseband and, in conjunction with a suitable gain-programmable input stage, drives the front-end analogue AGC. It also has circuitry for eliminating DC offsets and IQ imbalances.

The **Decimator (DEC)** block can be programmed to provide sample-rate decimation factors of between 1 and 4096, in octave steps.

The **Timing Recovery (TIM)** block uses an interpolating filter to resample the input signal at the symbol rate. This resampled input is then filtered using a root raised cosine matched filter.

The **Blind Adaptive Equaliser (AEQ)** is an optional block* which implements an N stage (where N = 2M+1 (1 Ò M Ò 7)) linear transversal filter to significantly reduce the effect of certain channel induced distortions, such as multipath.

The **Carrier Recovery (CARS)** block implements carrier recovery, carrier rotation and coherent gain functions, so that the incoming symbol points fall on the nominal constellation points.

The **Finite State Machine (FSM)** block controls the demodulator and schedules the procedures for acquisition, tracking, and reacquisition.

The **Simple Microprocessor Interface (SMPI)** block controls the microprocessor interface to the demodulator register set. It utilizes a conventional single transaction DTREQ/DTACK handshake protocol.

**HDRM-D2 core only*

Deliverables

There are four licensing models for this IP core (each with a royalty-free and a royalty-based variant):

- Single-Project Netlist (project-based, FPGA-specific)
- Multi-Project Netlist (site-based, FPGA-specific)
- Multi-Project VHDL (site-based, source-code)
- Multi-Project VHDL & C (site-based, full-capability)

The "full-capability" option provides all the VHDL source code, C models and MATLAB® models. It also includes additional documentation which details the algorithms used in the design, allowing fine tuning of system performance. FPGA-specific netlists are available for multiple vendors, including Xilinx, Altera and Lattice.

Deliverables	
Documentation	Hardware guide Programming guide Simulation guide Architectural overview* Advanced programming guide* *Full capability licence only*
Design Formats	Technology specific netlist VHDL source* MATLAB® Model** *Source & full capability licences **Full capability licence only*
Constraints	FPGA constraints guide file
Verification	VHDL verification testbench
Templates	VHDL & verilog instantiation templates

Support
3 months support included

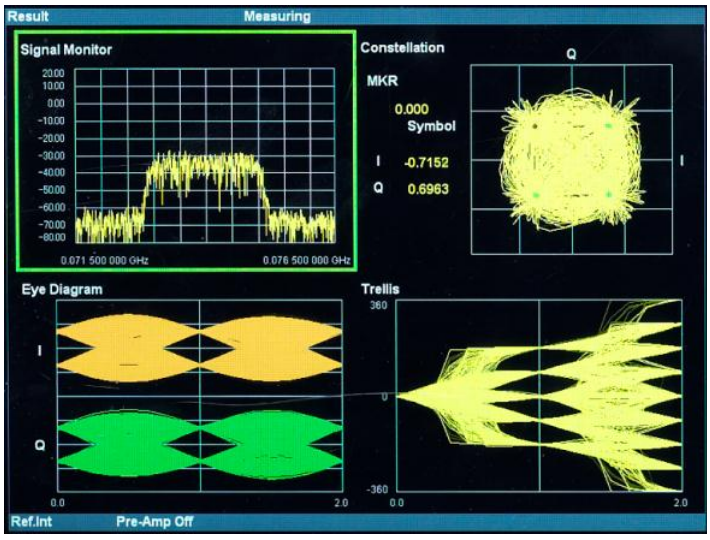
Additional Products

Zaltys Related Cores

The Zaltys High Data Rate Modulator (HDRM-M) IP core is a high performance modulator and is the natural partner for the HDRM-D and HDRM-D2 cores.

Zaltys MPE adapters enable Ethernet and other data services to be connected to our range of modulators and demodulators to provide high data rate communication links. The Zaltys MPE Encapsulator core (MPE-E) encapsulates high rate Ethernet and arbitrary data streams in a transport stream so they can be input to a modulator (such as the Zaltys HDRM-M) for transmission. At the receiver, a demodulator (such as the Zaltys HDRM-D) recovers the transport stream and the Zaltys MPE Decapsulator core (MPE-D) recreates the original Ethernet and other data streams.

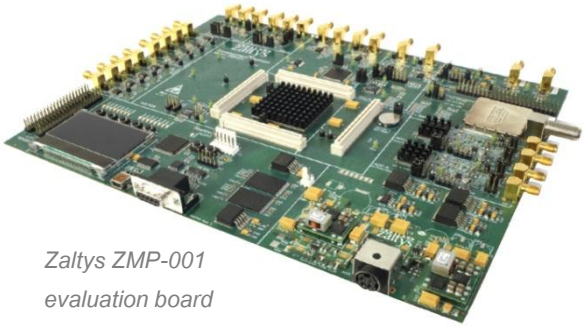
Silicon Infusion also supplies many other communications-related cores to help complete your design, including our High Data Rate modulator and demodulator cores (HDRM range), DVB-S and DVB-S2 solutions and Intelsat related framing and FEC solutions. Please contact us with your enquiry.



High Data Rate Demodulator Core

Zaltys Evaluation Boards

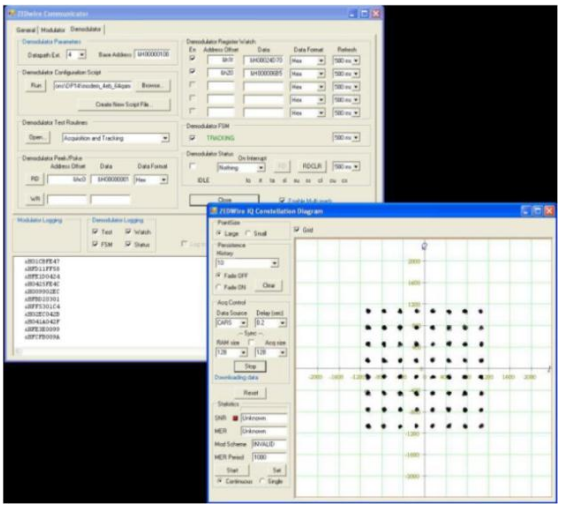
Evaluation boards are available for Zaltys products including the HDRM-D and HDRM-D2 cores. They connect to a PC via a USB or serial port, allowing easy communication with the ZEDwire Communicator software.



Zaltys ZMP-001 evaluation board

Zaltys GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the Zaltys evaluation boards, enabling rapid testing and evaluation of Zaltys cores.



ZEDwire Communicator Software

About Silicon Infusion and Zaltys

Silicon Infusion has been established for over ten years, and has a successful history of providing unique and innovative technical solutions to the wireless telecommunications industry. Our global client list includes organisations from many diverse market sectors - from Broadcast and Telecoms equipment manufacturers to Military solutions providers.

The Zaltys range of products are used for efficient high-speed transmission of voice, video and data. Zaltys modem cores are currently being used in many third-party products, carrying many thousands of user connections on a daily basis.

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