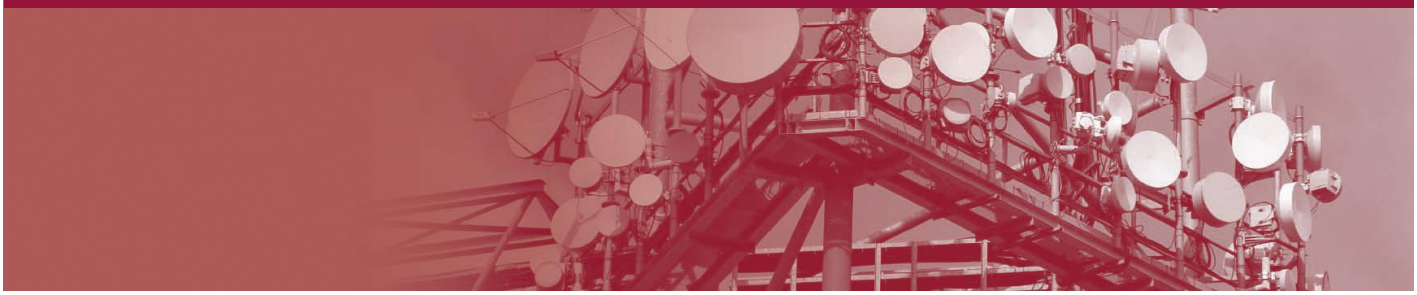
High Data Rate Modulator HDRM-M

Product Overview



Features

- Versatile digital modulation engine
- Programmable constellation mapper supports multiple constellations from BPSK to 256QAM
- Supports offset QPSK (OQPSK)
- Supports continuously variable symbol rates
  - Internal filter interpolates up to a factor of 8192
  - Supports typical rates of 2.5kbaud to 40Mbaud with 100MHz clock (range scales linearly with clock)
- Built-in transmit symbol rate NCO
  - FLL (frequency-locked-loop) allows transmit symbol rate to be locked to an external reference
- Matched filter with fully programmable alpha from 20% upwards
- Programmable 2's complement or offset-binary 8, 10, 12 or 14-bit DAC I & Q interfaces
- Versatile FIFO input accepts n-bit symbols ($1 \le n \le 8$) or raw I /Q constellation point coordinates
- Built-in sin(x)/x DAC compensation filters and internal gain and offset calibration
- Highly configurable and versatile
  - Fully programmable via microprocessor interface
- Simple microprocessor interface (SMPI)
- Suitable for FPGA or ASIC implementation
  - Xilinx Virtex®-6 implementations support over 100Mbaud (800Mb/s throughput with 256QAM
- Synchronous design with single clock
- Hardware evaluation board (available extra)

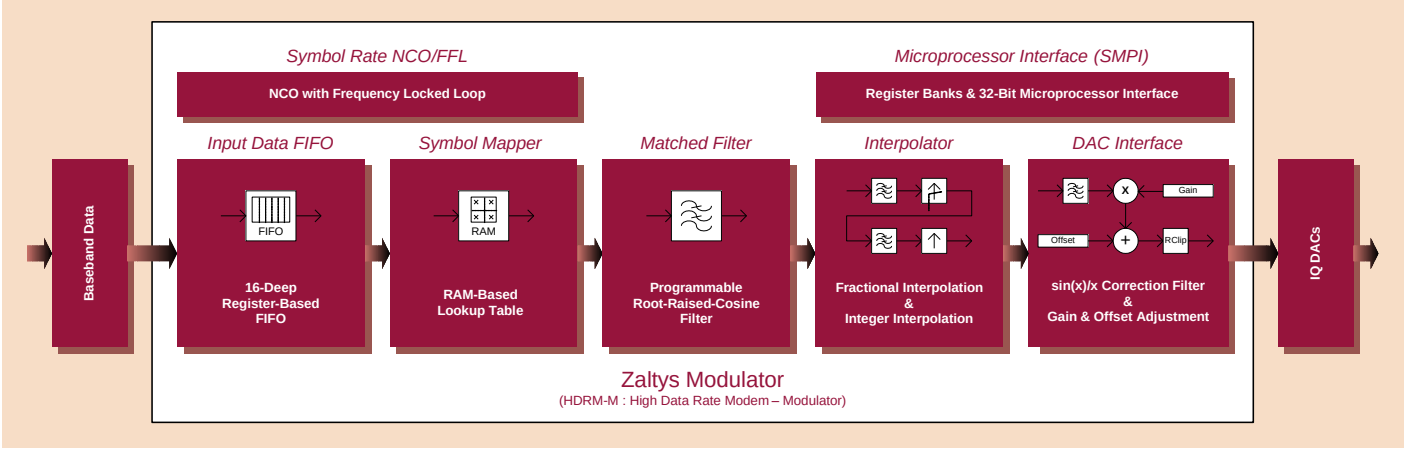
Introduction

The Zaltys High Data Rate Modulator (HDRM-M) IP core efficiently realizes the digital baseband section of a high performance modem transmit path, including symbol-mapping, matched filtering, sample interpolation, and DAC interfacing. Using sophisticated DSP techniques, the core can generate any modulation scheme up to 8 bits wide, such as (but not restricted to) BSPK, QPSK, 8QAM, 16QAM, 32APSK, 64QAM, 128QAM and 256QAM, all to a high performance level and at high symbol rates. The modulator is highly flexible, supporting continuously variable software-selectable symbol rates of between 2.5kbaud and 40Mbaud, when operating with a fixed 100MHz system/DAC clock rate. This is the typical performance achievable when implementing the design using inexpensive FPGA devices, but increased data rates are possible by targeting the design to higher performance FPGA families which allow an increase in system clock rate. Once configured via the 32-bit microprocessor interface, the modulator operation is completely automatic.

The HDRM-M core is ideally suited to point-to-point wireless applications such as satellite communications and microwave line-of-sight backhaul links (e.g. cellular, broadband or WiMAX). It also has applications in wired and optical links.

Technical Overview

Raw data is mapped to IQ constellation points by the mapper. Alternatively, the modulator can be supplied directly with the IQ constellation points. The mapped symbols are then passed through a programmable matched filter, before being interpolated up to the DAC sample rate. A built-in FLL allows the symbol rate to be locked to an external reference.



High Data Rate Modulator HDRM-M

Product Overview

Technical Overview continued

Modulator Architecture

The modulator datapath consists of five distinct sections. These correspond to the Input Data FIFO, Symbol Mapper, Matched Filter, Interpolator and DAC Interface functions. System timing is controlled by an integrated Symbol Rate NCO/FLL. Communications with the core is handled by a 32-bit Simple Microprocessor Interface.

Input Data FIFO

This block provides a small sixteen word input FIFO for accepting transmit data, either in the form of n-bit symbols ($1 \le n \le 8$) or raw I/ Q constellation points.

Symbol Mapper

This block maps symbol inputs to I and Q constellation points using a RAM based look-up table, which is fully programmable via the microprocessor interface. It supports a huge set of modulation schemes, including offset QPSK and asymmetrical schemes (NS-nQAM).

Matched Filter

Mapped symbols are passed through an RRC filter, which can support excess bandwidths of 20% or greater. It is fully programmable via the microprocessor interface.

Interpolator

This block matches the data to the DAC conversion rate, by using a fractional interpolation filter followed by an integer interpolation filter, up to a factor of 8192.

DAC Interface

The modulated output can be gain and offset calibrated, and a DAC compensation filter is available to compensate for sin(x)/x roll-off. The final output takes the form of I and Q sample pairs suitable for passing to high conversion rate 8, 10, 12 or 14 bit DACs.

Symbol Rate NCO/FLL

This block controls the rate of data flow through the modulator. The Symbol Rate NCO can be configured as a free-running, or can be locked to an external reference signal using the Symbol Rate FLL.

Simple Microprocessor Interface (SMPI)

This block controls the microprocessor interface to the modulator register set. It utilizes a conventional single transaction DTREQ/DTACK handshake protocol.

Deliverables

There are four licensing models for this IP core:

- Single-Project Netlist (project-based, FPGA-specific)
- Multi-Project Netlist (site-based, FPGA-specific)
- Multi-Project VHDL (site-based, source-code)
- Multi-Project VHDL & C (site-based, full-capability)

The "full-capability" option provides all the VHDL source code, C models and MATLAB® models. It also includes additional documentation which details the algorithms used in the design, allowing fine tuning of system performance. Site based licenses can be used in multiple projects. FPGA-specific netlists are available for multiple vendors, including Xilinx, Altera and Lattice.

Deliverables	
Documentation	Hardware Guide Programming Guide Simulation Guide Architectural Overview* Advanced Programming Guide* **full capability licence only*
Design Formats	Technology Specific Netlist VHDL Source* MATLAB® Model** **source & full capability licences* ***full capability licence only*
Constraints	FPGA Constraints Guideline File
Verification	VHDL Testbench
Templates	VHDL & verilog Instantiation Templates
Support	
3 Months Support Included	

Additional Products

Zaltys Evaluation Board (ZMP-001)

This board is designed to demonstrate Zaltys products, including the HDRM-M, at rates of over 65Mbaud. The board uses Xilinx Virtex-4 technology, and can be fitted

with custom daughterboard's to extend its functionality. It connects to a PC via a USB or serial port, allowing easy communication with the ZEDcommunicator software.

Zaltys ZMP-001 GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the ZMP-001 board, allowing rapid evaluation of Zaltys cores.

Related Cores

The Zaltys High Data Rate Demodulator (HDRM-D) IP core forms the digital baseband section of a high performance modem receive path, including quasi-zero IF to baseband conversion, sample decimation, symbol timing recovery, and carrier recovery. The core can demodulate BPSK, QPSK, offset-QPSK (OQPSK), 8PSK and 16QAM, all at high symbol rates.

The Zaltys High Data Rate Enhanced Demodulator (HDRM-D2) IP core adds support for 8QAM (3 shapes), 64QAM, 16APSK and 32APSK, and comes with an integral blind adaptive equaliser. It also supports an increase in datapath resolution up to 14-bits, which allows it to cope with higher levels of adjacent channel interference.

Silicon Infusion also supplies many other related cores to help complete your design, such as DVB and Intelsat related framing and FEC solutions. Please contact Silicon Infusion with your enquiry.

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