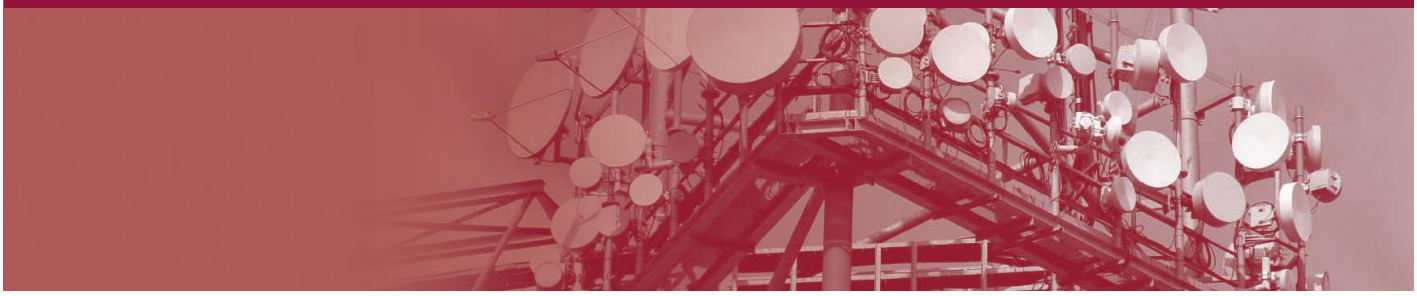
3-Layer ISDB-T Modulator (ISDBT-M)

Product Overview



Features

- Full 13-segment ISDB-T modulator
- 1 or 3-layer options (3-layers allow 2-layer operation)
- ARIB STD-B31 compliant (excluding Multiplex)
- Transport-stream interface for each supported layer
- Supports 2K, 4K & 8K FFT sizes (modes 1, 2 & 3)
- DQPSK, QPSK, 16QAM & 64QAM modulation schemes
- Separate TMCC & AC1/AC2 channel input ports both support dynamic operation
- Microprocessor controllable via SPI interface
- Two SDR SDRAM interfaces
  - Interleaver (only needed for timing interleaver)
  - Layer alignment (only needed for 3-layer operation)
- 1, 2, 4, 8, 16 & 32 timing interleaver depths
- 1/2, 2/3, 3/4, 5/6 & 7/8 code rates
- 1/4, 1/8, 1/16 & 1/32 guard intervals
- Time windowing reduces effects of OFDM symbol discontinuities
- Test-mode traffic generator
- Fully synchronous design
  - System clock depends on transmission bandwidth
    - (4096/63) MHz for 6MHz bandwidth
    - (2048/27) MHz for 7MHz bandwidth
    - (16384/189) MHz for 8MHz bandwidth
  - Parallel layer interface clock(s)
    - Separate interface clock per supported layer
- Suitable for Xilinx FPGA only
  - Needs Xilinx FFT core generated in Xilinx CoreGen
  - Other FPGA & ASIC vendors supported on request
- Hardware evaluation board (available extra)

Introduction

The Zaltys Terrestrial Integrated Services Digital Broadcasting (ISDBT-M) IP core efficiently realizes the digital baseband transmission functions as described in ARIB STD-B31. The core can process one MPEG transport-stream per supported-layer, and performs all the necessary processing required to output a complex baseband signal to a pair of external DACs.

The bandwidth of the generated signal is directly related to the supplied system clock, as per the table below. One sample is sent to the external DACs every eight system clock cycles.

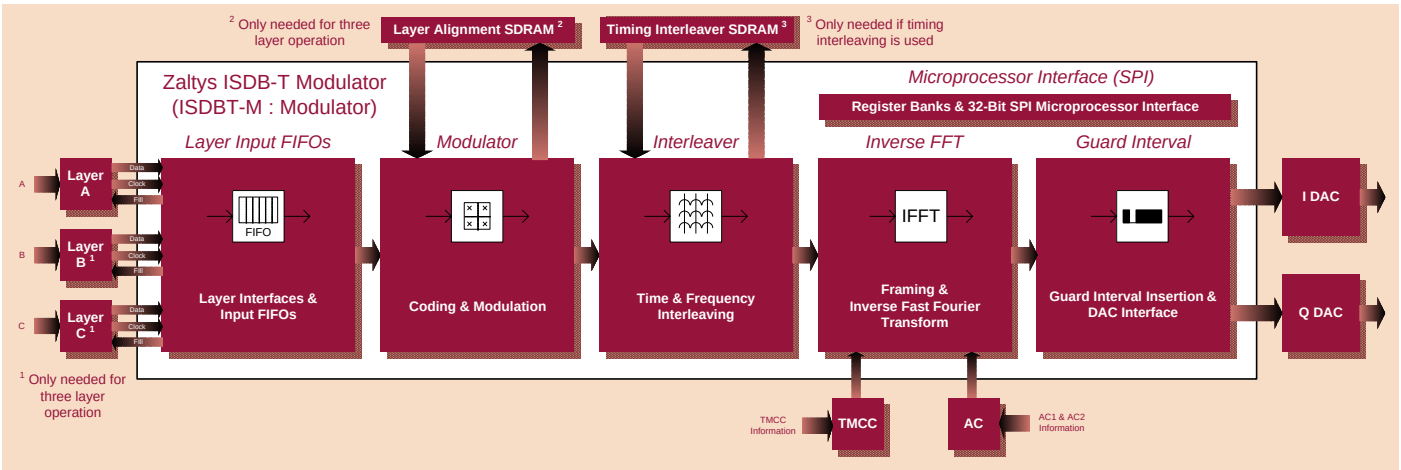
Transmission Bandwidth	System Clock (MHz)
6 MHz	4096/63 (65.01587…)
7 MHz	2048/27 (75.85185…)
8 MHz	16384/189 (86.68783…)

Two external SDRAM devices are required, one for time-interleaving and the other for multiple layer operation. If either or both of these features are not required, then the corresponding SDRAM(s) may be omitted. Each SDRAM device should be compatible with an ISSI IS42S16400D-7TL 64Mbit synchronous DRAM (1 Mbit x 16 bit x 4 banks).

The ISDBT-M core is ideally suited to applications such as broadcast digital television, mobile television cameras, and outside broadcast units.

Technical Overview

The incoming transmit transport streams enter individual input FIFO buffers, one per layer. Each layer has a specific error correction code rate, modulation scheme, and time-interleaver depth applied to it. The resulting data is frequency-interleaved. Pilot carriers are then added, along



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Product Overview

Technical Overview continued

with configuration control information (TMCC) and auxiliary channel information (AC1 & AC2). The resulting segment frame is passed through an IFFT block, and a programmable guard interval is copied into the result before it is sent to the external I & Q DACs.

Modulator Architecture

Layer Input FIFOs

Up to three 1023-byte input FIFO buffers (one per supported layer) hold the incoming MPEG transport-streams before they are consumed by the internal processing blocks. FIFO level signals allow external circuitry to ensure that any particular FIFO does not underflow or overflow, thus facilitating transport-stream rate adaptation. Synchronisation bytes are automatically detected for each layer, ensuring correct byte alignment.

Coding & Modulation

This block is replicated for each supported layer. It takes the MPEG packets and adds a Reed Solomon outer code, followed by energy dispersal, delay adjustment and byte wise interleaving. It then adds a convolutional inner code, with each supported layer having its own unique code rate. Further delay adjustment is applied before performing a bit-interleave operation and mapping the resulting data to I & Q constellation points, with each supported layer having its own unique modulation type.

Time & Frequency Interleaving

Each supported layer is assigned a single or group of segments to transport it. The segments corresponding to each supported layer are time-interleaved according to the depth parameter for that particular layer. The segments are then split into portions depending on whether they are associated with partial reception, coherent modulation, or differential modulation. Each individual segment corresponding to the differential and coherent portions is then frequency-interleaved within itself. The individual groups of segments corresponding to partial reception, coherent modulation, or differential modulation are then frequency-interleaved within themselves by performing a carrier rotation followed by a carrier randomisation.

Framing & IFFT

The interleaved data is combined with pilot tones, TMCC information, and the AC channels to form the OFDM segment frame. The frame makeup differs depending on whether differential or coherent modulation is present in the segment. The 13-segments are then ordered, a continual pilot tone is added to the higher edge of the band, and the whole configuration is sent to a complex 2K, 4K or 8K IFFT to generate the OFDM symbols.

Guard-Interval Insertion & DAC Interface

After the IFFT, a guard interval is inserted into the data stream by concatenating samples copied from the end of the IFFT result onto the front of the IFFT result. The final output takes the form of I & Q sample pairs suitable for passing to a pair of 14-bit DACs.

Deliverables

There are three licensing models for this IP core:

- Single-Project Netlist (project-based, Xilinx-specific)
- Multi-Project Netlist (site-based, Xilinx-specific)
- Multi-Project VHDL (site-based, full-capability)

Site based licenses can be used in multiple projects.

Deliverables	
Documentation	Hardware & Programming Guide
Design Formats	Xilinx Technology Specific Netlist VHDL Source *(source licences only)*
Constraints	FPGA Constraints Guideline File
Verification	VHDL Testbench
Templates	VHDL & verilog Instantiation Templates
Support	
3 Months Support Included	

Additional Products

Zaltys Evaluation Board (ZMP-001)

This board is designed to demonstrate Zaltys products, including the ISDB-T core. The board uses Xilinx Virtex-4 technology, and can be fitted with custom daughterboard's to extend its functionality.

It connects to a PC via a USB or serial port, allowing easy communication with the ZEDcommunicator software.

Zaltys ZMP-001 GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the ZMP-001 board, allowing rapid evaluation of Zaltys cores.

Related Cores

The Zaltys High Data Rate Enhanced Demodulator (HDRM-D2) IP core forms the digital baseband section of a high performance modem receive path, including quasi-zero IF to baseband conversion, sample decimation, symbol timing recovery, blind adaptive equalisation, and carrier recovery. The core supports multiple schemes, from BPSK to 256QAM, all at high symbol rates. Increased data resolution also allows it to cope with high levels of adjacent channel interference.

The Zaltys High Data Rate Modulator (HDRM-M) IP core forms the digital baseband section of a high performance modem transmit path, including symbol-mapping, matched-filtering, interpolation, and DAC interfacing.

Silicon Infusion also supplies many other related cores to help complete your design, such as DVB and Intelsat related framing and FEC solutions. Please contact Silicon Infusion with your enquiry.

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