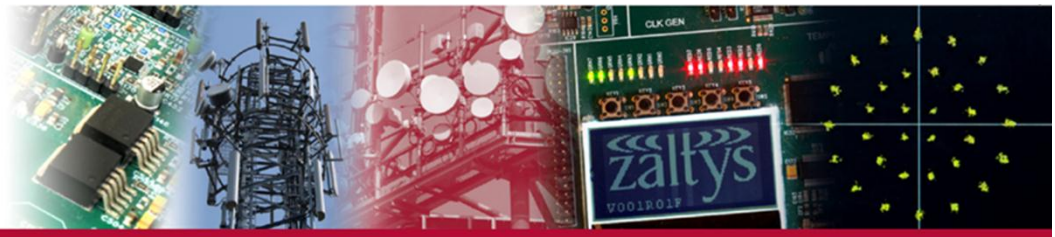


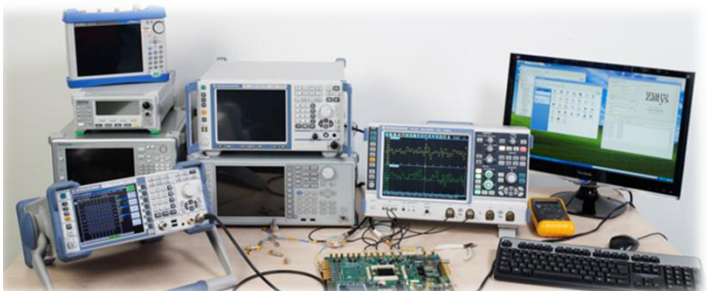
ZnZ Evaluation Board ZNZ-001

Introduction

The Zaltys ZnZ Evaluation Board (ZNZ-001) is designed to allow our customers to easily instantiate and evaluate the performance of our Zaltys range of communications IP cores. The board contains two Xilinx FPGA devices, each capable of running many of our current Zaltys range of IP cores. For example, a Zaltys modulator core can run on one Xilinx while a complementary Zaltys demodulator core is run on the other, facilitating back-to-back performance testing of a complete modem. Each FPGA has its own DDR memory, allowing cores which incorporate memory-intensive algorithms to be accommodated with ease.

Naturally, our customers are free to instantiate their own designs within the two Xilinx FPGAs, in conjunction with Zaltys cores if they so require. Customer designs are able to access the many on-board communications-related features of the evaluation board, such as the 16-bit dual DAC and ADC, the analogue modulator and demodulator, the 10/100/1G Ethernet interfaces, the MPEG ASI transceivers, and the plentiful general-purpose digital I/O. The board also incorporates two FMC connectors for easy connection of expansion and 3rd party FMC modules.

The Zaltys ZnZ evaluation board is a powerful environment for customer product development. Indeed some customers may prefer to use the ZNZ-001 board directly in their products rather than designing their own PCBs.



Features

- Ideal evaluation platform for the full range of Zaltys communications IP cores
- Incorporates two Xilinx FPGA devices – enough power to easily run both a modulator and a demodulator core simultaneously
- ARM Cortex based CPU handles loading of cores into Xilinx devices and subsequent configuration and interaction with the cores
- On board FLASH memory to store CPU code and core bit files locally – enables board to autonomously boot from power-up to a fully configured and operating modem with no external interaction
- On board 16-bit dual DAC and ADC (with associated filters) for complex baseband (I/Q) I/O
- On board RF modulator and demodulator for RF I/O
- Industry standard headers provide plenty of I/O for digital data streams (e.g. MPEG transport streams)
- Four on board MPEG ASI transceivers
- Each Xilinx is connected to its own 64Mbyte DDR memory device supporting memory intensive applications such as de-interleaving or SFN delay adjustment
- Two FMC connectors to accommodate expansion modules (e.g. alternative radios, ADCs, DACs, CPUs, I/O breakout, etc.) conforming to the industry standard FMC spec
- One RS232 interface
- Two USB interfaces
- Three 10/100/1G Ethernet interfaces
- GPS time reference input for SFN applications
- Flexible system clock management provides several fixed frequencies & two programmable frequency synthesisers

PRELIMINARY INFORMATION - SUBJECT TO CHANGE
PRODUCT EXPECTED Q1 2012

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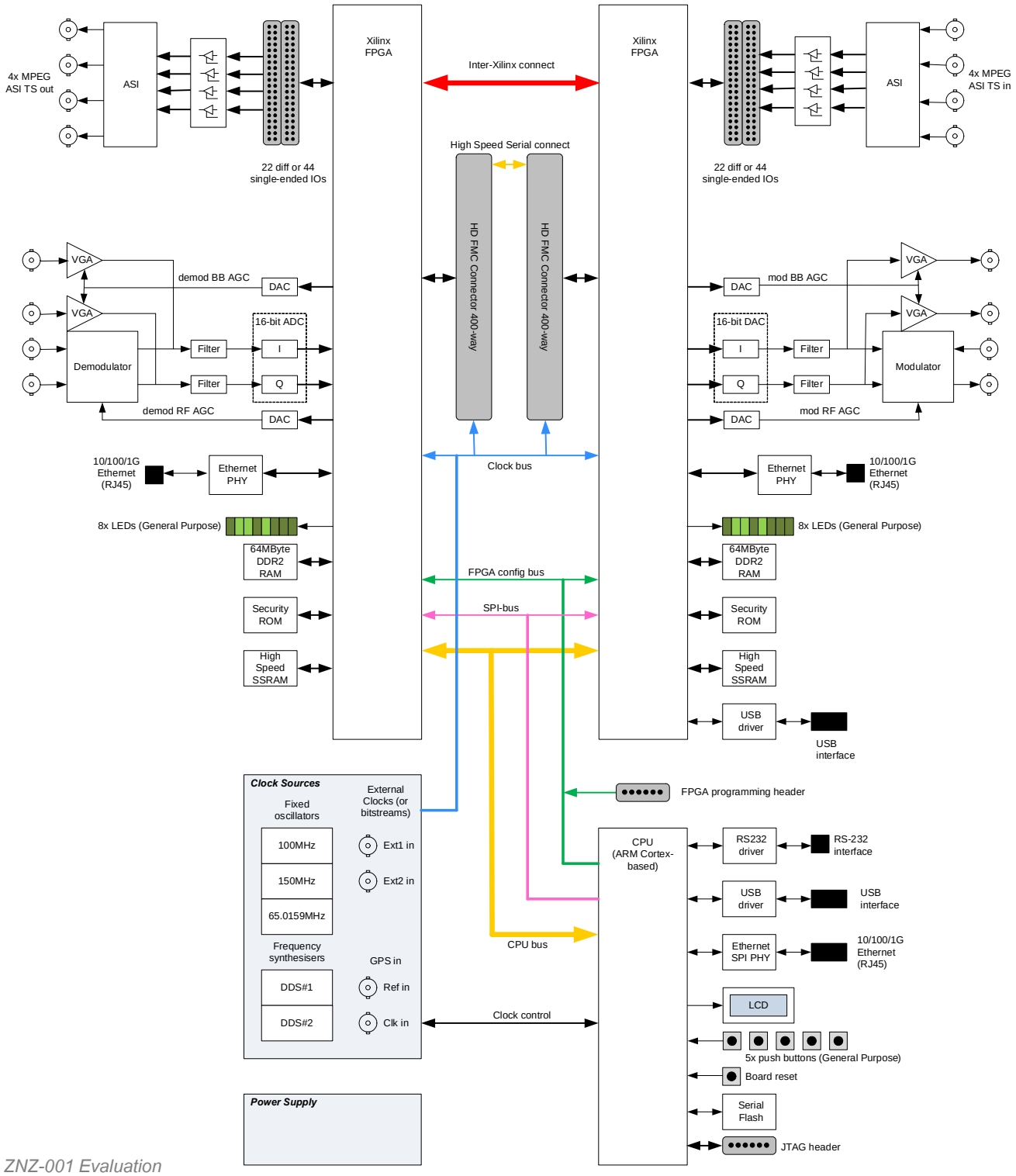
ZnZ Evaluation Board



ZNZ-001 Evaluation Board Block Diagram

Technical Overview

A dual 16-bit DAC with associated variable-gain amplifiers and filters is coupled to one FPGA enabling a modulator core to provide a standard I/Q output to a suitable transmitter. Additionally, an on-board analogue modulator can generate an RF output directly if desired. The other FPGA has a dual 16-bit ADC with associated variable-gain amplifiers and filters enabling baseband I/Q signals from a suitable radio receiver to be input to a demodulator core. As per the transmit direction, an on-board analogue demodulator can accept an RF input directly if desired. Of course the I/Q (or RF) output of the modulator may be connected directly to the I/Q (or RF) input of the demodulator for back-to-back performance testing.

A number of industry standard headers provide plenty of input and output connectivity to convey digital data for transmission to a modulator core, and to output received digital data from a demodulator core. These may be parallel or serial, single-ended or differential data streams, MPEG transport streams, or proprietary data streams. On-board transceivers enable MPEG ASI format transport streams to be directly interfaced.

Each FPGA is provided with a 10/100/1000Mbps Ethernet PHY and connector. Hence products providing point-to-point Ethernet links can be prototyped and evaluated.

Two VITA 57.1 FMC connectors are provided, one connected to each FPGA. These facilitate connection of daughter cards to expand the capabilities of the ZNZ-001 board by adding further FPGAs, CPUs, memory, data interfaces or a growing number of third-party communications-related, FMC-standard boards.

A high speed SSRAM device connected to each FPGA augments the SRAM integrated within the FPGA which can often prove rather limited in communications applications.

An ARM-Cortex-based CPU (the Cypress pSoC5 CPU) is responsible for configuring the board on power-up. Typically, the CPU will connect to a PC running our ZEDwire Communicator software enabling a user to load the FPGAs with the Zaltys cores of interest and configure them for operation. Naturally, the user is free to program the CPU for their own purposes. Enough FLASH storage is provided to hold the CPU software as well as a number of FPGA cores in “bit-file” format. An on-board LCD and 5-push buttons can be used to provide a simple user interface without the connection of an external PC if desired. The CPU has direct connection to USB, RS-232, and 10/100/1000 Ethernet interfaces.

A generous number of uncommitted digital data busses and high speed serial links connect FPGAs, FMC slots and CPU permitting large volumes of data to be transferred between devices. This facilitates schemes in which one device is used as a co-processor for another, or where a device wishes to make use of a peripheral or communications port attached to another device.

A clock management block provides system clocks to the FPGAs. It is controlled via the CPU and provides three fixed and two programmable clock frequencies.

ZnZ Evaluation Board

Additional Products

Zaltys Related Cores

The Zaltys 3-Layer ISDB-T Modulator (ISDBT-M) and Demodulator (ISDBT-D) are efficient, high-performance, ARIB STD-B31 compliant IP cores for use in Terrestrial Integrated Services Digital Broadcasting applications.

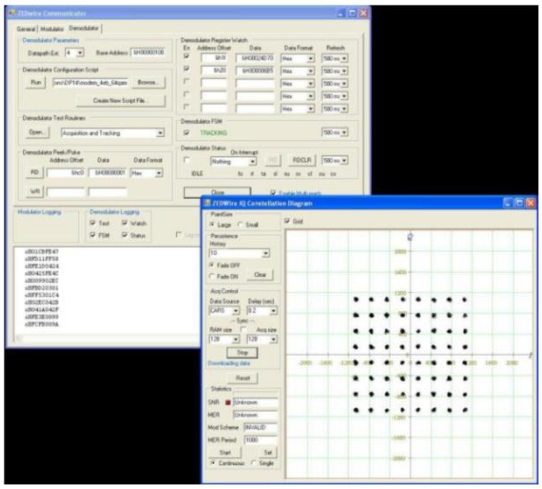
The Zaltys DVB-S2 Modulator (DVBS2-M) and Demodulator (DVBS2-D) are high-performance IP cores for use in DVB-S2 applications.

The Zaltys High Data Rate Modulator (HDRM-M) and Demodulator (HDRM-D & HDRM-D2) IP cores are powerful general purpose solutions for a wide range of digital communications applications. These cores can support many modulation schemes, including BPSK, QPSK, OQPSK, 8PSK, 8/16/32/64QAM and 16/32APSK.

Silicon Infusion also supplies many other communications-related cores to help complete your design. Please contact Silicon Infusion with your enquiry.

Zaltys GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the Zaltys evaluation boards, enabling rapid testing and evaluation of Zaltys cores.



Zaltys ZEDwire Communicator software

About Silicon Infusion and Zaltys

Silicon Infusion has been established for over ten years, and has a successful history of providing unique and innovative technical solutions to the wireless telecommunications industry. Our global client list includes organisations from many diverse market sectors - from Broadcast and Telecoms equipment manufacturers to Military solutions providers.

The Zaltys range of products are used for efficient high-speed transmission of voice, video and data. Zaltys modem cores are currently being used in many third-party products, carrying many thousands of user connections on a daily basis.

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